IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Alfredo Herrera	Examiner:	Unassigned
Serial No.:	Unassigned	Art Unit:	Unassigned
Filed:	Herewith	Attorney Docket No.:	16550ROUS01U
Title:	METHOD AND APPARATUS FOR AUTOMATING THE DESIGN OF PROGRAMMABLE LOGIC DEVICES		

M.S. Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicant respectfully submits for consideration the references identified on the enclosed PTO-1449, and requests that the Examiner return an initialed copy of the PTO-1449 to applicant with the next communication.

No fees are believed due in connection with this filing. If any fees are due in connection with this filing, the Commissioner is hereby authorized to charge payment of the fees associated with this communication or credit any overpayment to Deposit Account No. 502246 (Ref. NN-16550).

Respectfully Submitted

Dated: February 4, 2004

John C. Gorecki
Registration No. 38,471

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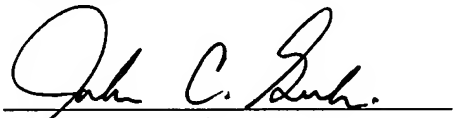

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Substitute for Form 1449A/PTO	Application No.	Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing Date	
	First Named Inventor	Alfredo Herrera
	Art Unit	Unknown
	Examiner	Unknown
Sheet 1 of 1	Attorney Docket No.	16550ROUS01U

U.S. PATENT DOCUMENTS				
Examiner's Initials	Citation Number	Document Number	Publication Date	Name of Patentee or Applicant of Cited Document
	A1			
	A2			
	A3			

FOREIGN PATENT DOCUMENTS				
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	B1			
	B2			

OTHER PRIOR ART -- NON-PATENT LITERATURE DOCUMENTS		
Examiner's Initials	Citation Number	Document Description -- Include the name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
	C1	*Field Programmable Gate Arrays An Enabling Technology*, (11 pages)
	C2	S. Lorenzini, *FPGA Design Cycle Time Reduction and Optimization*, (2 pages)
	C3	J. Ma, et al., *Incremental Design Techniques for Million-Gate FPGAs*, VTIP Disclosure No.: 01-110 (1 page)
	C4	*Xilinx Design Reuse Methodology for ASIC and FPGA Designers*, (27 pages)

Examiner Signature		Date Considered	

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute for Form 1449A/PTO	Application No.	Unknown
# INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing Date	
	First Named Inventor	Alfredo Herrera
	Art Unit	Unknown
	Examiner	Unknown
Sheet 1 of 1	Attorney Docket No.	16550ROUS01U

U.S. PATENT DOCUMENTS				
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	A1			
	A2			
	A3			

FOREIGN PATENT DOCUMENTS				
Examiner's Initials	Citation Number	Document Number	Publication Date	Name of Patentee or Applicant of Cited Document
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	B2			

OTHER PRIOR ART -- NON-PATENT LITERATURE DOCUMENTS		
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